

**PATENT APPLICATION**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

In re application of

Docket No: Q66664

Keld LANGE, et al.

Appln. No.: 09/981,784

Group Art Unit: 2617

Confirmation No.: 6691

Examiner: Sam BHATTACHARYA

Filed: October 19, 2001

For: BASE STATION OF A RADIO-OPERATED COMMUNICATIONS SYSTEM

**SUBMISSION OF APPEAL BRIEF**

**MAIL STOP APPEAL BRIEF - PATENTS**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

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Respectfully submitted,



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WASHINGTON OFFICE

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**APPEAL BRIEF UNDER 37 C.F.R. § 41.37**

**MAIL STOP APPEAL BRIEF - PATENTS**

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 37 C.F.R. § 41.37, Appellant submits the following:

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APPEAL BRIEF UNDER 37 C.F.R. § 41.37  
U.S. Appln. No. 09/981,784  
Attorney Docket No.: Q66664

**I. REAL PARTY IN INTEREST**

The real party in interest is ALCATEL, by virtue of an assignment recorded by the Assignment Branch of the U.S. Patent and Trademark Office on October 19, 2001, at Reel 012277, Frame 0169.

APPEAL BRIEF UNDER 37 C.F.R. § 41.37  
U.S. Appl. No. 09/981,784  
Attorney Docket No.: Q66664

## **II. RELATED APPEALS AND INTERFERENCES**

To the knowledge and belief of Appellant, the Assignee, and the undersigned, there are no other appeals or interferences before the Board of Appeals and Interferences that will directly affect or be affected by the Board's decision in the instant Appeal.

APPEAL BRIEF UNDER 37 C.F.R. § 41.37  
U.S. Appl. No. 09/981,784  
Attorney Docket No.: Q66664

### **III. STATUS OF CLAIMS**

Claims 1-16 and 19-24 are all the claims pending in the application. Claims 1-16 and 19-24 are rejected under 35 U.S.C. § 103(a). The rejected claims 1-16 and 19-24 are being appealed.

APPEAL BRIEF UNDER 37 C.F.R. § 41.37  
U.S. Appl. No. 09/981,784  
Attorney Docket No.: Q66664

#### **IV. STATUS OF AMENDMENTS**

With the filing of this Brief, all Amendments have been entered and considered by the Examiner.

The Appendix included with this Brief sets forth the claims involved in the appeal and reflects all of the claim amendments that have been entered by the Examiner.

## **V. SUMMARY OF THE CLAIMED SUBJECT MATTER**

In general, Appellant's invention relates a receiver that needs to perform chip rate processing and symbol rate processing.

In the background of the invention, it is disclosed that a conventional base station has a digital signal processor (hereinafter "DSP") for performing symbol rate processing and field programmable gate array (hereinafter "FPGA") for performing chip rate processing. The DSP cannot perform the chip rate processing and the FPGA cannot perform the symbol rate processing. When speech is transmitted, the data rate is low but the number of users can be high. Thus, a larger number of FPGAs is needed to perform the chip rate processing on the received speech. That is, the chip rate processing despreads or separates the speech of different users. When transmitting internet data, the data rate is high but the number of users is low. The internet data requires a high number of DSPs so as to perform the symbol rate processing. That is, since the data rate is high, there is more information to decode. The base station is equipped to accommodate both situations: when the number of users is high and when the data transmission rate is high. The two situations, however, will never occur simultaneously. Consequently, unused FPGAs or DSPs are always present in the base station of the conventional techniques (*see* page 1, line 24 to page 2, line 14 of the specification).

In an exemplary embodiment of the present invention, however, each digital signal processor can perform both: the symbol rate processing and the chip rate processing. Thereby, over-dimensioning of the base station is lessened. That is, the digital processor performs both symbol rate processing which is decoding of the received information and at least some of the chip rate processing. The chip rate processing is despreads or re-separating the transmitted

information of the different users in the receiver and assigning this information to the different users (*see* page 5, lines 21 to 31 of the specification). In other words, the received data is first despread (separated) and then decoded (*see* page 8, lines 19 to 30 of the specification).

Specifically, the base station 10 includes a signal processor 12 such as DSP that receives information 11. The signal processor 12 includes a programming module for chip rate processing 13 and a programming module for symbol rate processing 14. The signal processor further includes a programming module for task allocation 15. The task allocation programming module 15 defines the mode of operation of the signal processor 12, performs the switch-over between the chip rate processing and the symbol processing, controls forwarding of information that may be necessary for the switching, and receives feedback information from the chip rate programming module 13 and the symbol rate programming module 14 (*see* Figure and page 6, line 26 to page 8, line 4 of the specification).

In addition, a number of signal processors may be provided. These signal processors are split into subgroups, where one subgroup performs chip rate processing and another subgroup performs signal rate processing. In other words, both: the chip rate processing and the signal rate processing are performed in parallel by these subgroups (page 9, lines 6 to 31 of the specification).

Thereby, when speech is transmitted, more of the processors can be used for the chip rate processing and when Internet data is transmitted, more of the processors can be used for the symbol rate processing. Accordingly, the base station is more compact and resources are used more efficiently. In this base station, a single digital processor despreads as well as decodes the received information (*see* page 9, lines 1 to 31 of the specification).

Claim 1, for example, is directed to a base station of a radio-operated telecommunications system. The base station includes a receiver processing received information and one or more digital signal processors. Each of the digital signal processors is configured to perform a symbol rate processing and at least parts of a chip rate processing (*see* Fig and page 6, line 26 to page 8, line 4 of the specification).

Claim 5, for example, further recites: the chip rate processing and the symbol rate processing can be distributed between sub-arrays or sub-groups of signal processors (*see* page 9, lines 6 to 31 of the specification).

Claim 9, for example, is directed to a receiver for a base station of a radio-operated telecommunications system. The receiver processes received information with one or more digital signal processors. Each of the digital signal processors is configured for performing a symbol rate processing and at least parts of a chip rate processing (*see* Fig and page 6, line 26 to page 8, line 4 of the specification).

Claim 10, for example, is directed to a digital signal processor configured to execute symbol rate processing for a receiver of a base station of a radio-operated telecommunications system. The signal processor is configured to perform at least parts of a chip rate processing (*see* Fig and page 6, line 26 to page 8, line 4 of the specification).

Claim 11, for example, is directed to a radio-operated telecommunications system. The system includes at least one of: a base station having one or more digital signal processors, a receiver processing received information having one or more digital signal processors, and one or more digital processors. Each of these digital signal processors is configured to perform a

symbol rate processing and at least parts of a chip rate processing (*see* Fig and page 6, line 26 to page 8, line 4 of the specification).

Claim 12, for example, is directed to a process for operating a radio-operated telecommunications system. The information received by a base station is subjected to a symbol rate processing by one or more digital signal processors. At least a part of the chip rate processing is performed by same processor from the digital signal processors (*see* Fig and page 6, line 26 to page 8, line 4 of the specification).

Claim 20, for example, is directed to a digital signal processor. The digital signal processor includes means for executing symbol rate processing, means for executing chip rate processing, and means for switching over from said means for executing symbol rate processing to said means for executing chip rate processing. This digital signal processor is a single digital processor having the symbol rate processing means, the chip rate processing means and the switching means. This digital signal processor is disposed inside a receiver (*see* Fig and page 6, line 26 to page 8, line 4 of the specification).

Claim 21 further recites that the means for switching instructs for transmission of information in the digital processor first to the means for executing chip rate processing and then to the means for executing symbol rate processing. That is, the task allocation 15 controls the signal processor so that chip rate processing 13 is performed and then the signal processor is controlled by the task allocation 15 so that symbol rate processing is performed (*see* Fig; page 7, line 21 to page 8, line 4 and page 8, lines 6 to 22 of the specification).

Claim 22 further recites that each of the digital signal processors is configured to perform the symbol rate processing comprising decoding the received information and at least parts of the

chip rate processing comprising despreading the received information (*see* Fig; page 7, lines 4 to 7 and page 5, line 21 to page 6, line 15 of the specification).

Claim 23 further recites that the despreading comprises separating the received information based on sources of the received information and assigning the separated received information to a respective source (*see* Fig; page 7, lines 4 to 7 and page 5, line 21 to page 6, line 15 of the specification).

Claim 24 further recites the symbol rate processing means decode the received information and wherein said chip rate processing means despread the received information (*see* Fig; page 7, lines 4 to 7 and page 5, line 21 to page 6, line 15 of the specification).

**VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL**

There are four issues on Appeal.

The first issue is whether claims 1, 3, 6-13, and 19 are improperly finally rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,366,606 to Sriram (hereinafter “Sriram”) in view of U.S. Patent No. 6,366,607 to Ozluturk et al. (hereinafter “Ozluturk”).

The second issue is whether claims 2, 14, and 16 are improperly finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Sriram and Ozluturk in view of U.S. Patent No. 4,827,499 to Warty (hereinafter “Warty”).

The third issue is whether claims 4, 5, and 15 are improperly finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Sriram, Ozluturk and Warty in view of U.S. Patent No. 6,161,024 to Komara (hereinafter “Komara”).

The fourth issue is whether claims 20-24 are improperly finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Ozluturk in view of U.S. Publication No. 2001/0034227 to Subramanian et al. (hereinafter “Subramanian”).

## **VII. ARGUMENT**

Appellant respectfully requests the Board to reverse the final rejections of the claims pending in the application for at least the following reasons.

### **Issue 1: Claims 1, 3, 6-13, and 19 are Patentable over Sriram in view of Ozluturk.**

Claims 1, 3, 6-13, and 19 are improperly finally rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,366,606 to Sriram (hereinafter “Sriram”) in view of U.S. Patent No. 6,366,607 to Ozluturk et al. (hereinafter “Ozluturk”).

#### ***i. Legal Standard***

The initial burden of establishing that a claimed invention is *prima facie* obvious rests on the USPTO. *In re Rikckaert*, 9 F.3d 1531, 1532 (Fed. Cir. 1993). To make its *prima facie* case of obviousness, the USPTO must satisfy three requirements:

- a) The prior art relied upon, coupled with the knowledge generally available in the art at the time of the invention, must contain some suggestion or incentive that would have motivated to artisan to modify a reference or to combine references. *In re Thrif*, 298 F.3d 1357, 1363 (Fed. Cir. 2002).
- b) The proposed modification of the prior art must have had a reasonable expectation of success, and that determined from the vantage point of the artisan at the time the invention was made. *Amgen, Inc. v. Chugai Pharm. Co.*, 927 F.2d 1200, 1209 (Fed. Cir. 1991).
- c) The prior art reference or combination of references must teach or suggest all the limitations of the claims. *In re Vaeck*, 20 U.S.P.Q.2d 1438, 1442 (Fed. Cir. 1991); *In re Wilson*, 424 F.2d 1382, 1385 (CCPA 1970).

The motivation, suggestion or teaching may come explicitly from statements in the prior art, the knowledge of one of ordinary skill in the art, or, the nature of a problem to be solved. *In re Dembiczak*, 175 F.3d 994, 999 (Fed. Cir. 1999). Alternatively, the motivation may be implicit from the prior art as a whole, rather than expressly stated. *Id.* Regardless if the USPTO relies on an express or an implicit showing of motivation, the USPTO is obligated to provide particular findings related to its conclusion, and those findings must be clear and particular. *Id.*

A critical step in analyzing the patentability of claims pursuant to section 103(a) is casting the mind back to the time of invention, to consider the thinking of one of ordinary skill in the art, guided only by the prior art references and the then-accepted wisdom in the field. *See In re Kotzab*, 55 USPQ2d 1313, 1316 (Fed. Cir. 2000) (*citing In re Dembiczak*, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999)). Close adherence to this methodology is especially important in cases where the very ease with which the invention can be understood may prompt one “to fall victim to the insidious effect of a hindsight syndrome wherein that which only the invention taught is used against its teacher.” *In re Kotzab*, 55 USPQ2d at 1316 (*quoting W.L. Gore & Assocs., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1553, 220 USPQ 303, 313 (Fed. Cir. 1983)).

***ii. Unique Features of Independent Claims 1 and 9-12***

Of these rejected claims, only claims 1 and 9-12 are independent. These independent claims 1 and 9-12, in some variation, *inter alia* require a digital processor that can perform both symbol rate processing and at least a portion of the chip rate processing.

That is, in an exemplary embodiment of the present invention, the digital processor performs both symbol rate processing which is decoding of the received information and at least

some of the chip rate processing. The chip rate processing is despreading or re-separating the transmitted information of the different users in the receiver and assigning this information to the different users (*see* page 5, lines 21 to 31 of the specification). Thereby, when speech is transmitted, more of the processors can be used for the chip rate processing and when Internet data is transmitted, more of the processors can be used for the symbol rate processing. Accordingly, the base station is more compact and resources are used more efficiently.

***iii. Prior Art References***

Sriram discloses a digital transmissions receiver system which includes a digital transmissions receiver and a correlation co-processor. The correlation co-processor performs correlation operations at the request of the digital transmissions receiver. Power consumption in the correlation co-processor is reduced by performing the requested correlation operations in stages. The number of stages used is inversely proportional to the number of gates required to implement the correlation function. Thus, the more stages used, the fewer gates are required. This, in turn, provides lower power consumption as compared with a non-staged implementation of the correlation function. Various types of correlations may be performed as indicated by correlation control signals received from the digital transmissions receiver. A correlation controller, included in the correlation co-processor, keeps track of the various stages and with the data appropriate to each stage. When all of the stages necessary to process a particular piece of data are complete, the recovered symbol rate data is stored in an output buffer to await symbol rate processing by the digital transmissions receiver (col. 1, lines 30 to 55).

In particular, Sriram discloses a digital receiver 10 (col. 2, lines 31 to 33). The digital receiver 10 interfaces with a programmable correlator co-processor 12, which is a separate unit

that communicates with the receiver. The correlator co-processor performs the chip rate processing using a chip correlator 34 (col. 2, lines 49 to 54; col. 3, lines 34 to 50). The receiver that includes a DSP (the digital processor) performs the symbol rate processing (Fig. 2; col. 5, lines 51 to 60).

Ozluturk relates to a digital spread spectrum communication system employing pilot-aided coherent multipath demodulation that effects a substantial reduction in global-pilot and assigned-pilot overheads (*see* Abstract). Specifically, Ozluturk discloses a receiver 29 that includes a demodulator 57a, 57b which mixes down the transmitted broadband signal 55 into an intermediate carrier frequency 59a, 59b. A second down conversion reduces the signal to baseband. The QPSK signal is then filtered 61 and mixed 63a, 63b with the locally generated complex pn sequence 43a, 43b which matches the conjugate of the transmitted complex code. Only the original waveforms which were spread by the same code at the transmitter 27 will be effectively despread. Others will appear as noise to the receiver 29. The data 65a, 65b is then passed onto a signal processor where FEC decoding is performed on the convolutionally encoded data (Fig. 2; col. 3, lines 41 to 53).

***iv. Examiner's Position***

The Examiner acknowledges that Sriram fails to disclose or suggest a single processor performing both the chip rate processing and the symbol rate processing (*see* page 2 of the Final Office Action). The Examiner, however, alleges that Ozluturk cures the deficient teachings of Sriram.

Specifically, the Examiner states that, in Ozluturk, “[t]here are no channel despanders in the embodiment shown in Fig. 2 and therefore both symbol rate and chip rate processing is

performed by the single signal processor 67” (see page 6 of the Office Action). The Examiner further notes that Figs. 12 and 13 disclose that symbol rate processing and chip rate processing are performed by the single processing unit 157 (see page 7 of the Office Action). In the Continuation Sheet of the Advisory Action mailed December 8, 2006, the Examiner maintains that the signal processor 67 of Ozluturk performs both chip rate processing and signal rate processing *i.e.*, the carrier offset correction may be performed at either levels by the signal processor.

The Examiner further notes that one of ordinary skill in the art would have been motivated to combine the processor of Ozluturk into the system of Sriram “to eliminate the unnecessary circuit components that previously performed the two kind of processing, and thereby save space by making the receiver circuitry more compact” (see page 2 of the Office Action).

***v. Appellant’s Position***

Appellant respectfully submits that the USPTO has not established a *prima facie* case of obviousness. The Examiner failed to satisfy the first and third requirements in establishing a *prima facie* case of obviousness. It is respectfully submitted that one of ordinary skill in the art would not have combined the references in the manner suggested by the Examiner without exercising impermissible hindsight. Furthermore, it is respectfully submitted that Ozluturk does not disclose or suggest a single processor performing both the symbol rate processing and at least a part of the chip rate processing.

***One of Ordinary Skill in the Art Would Not Have Combined Sriram with Ozluturk without Exercising Impermissible Hindsight***

The Examiner alleges that one of ordinary skill in the art would have been motivated to combine the processor of Ozluturk into the system of Sriram “to eliminate the unnecessary circuit components that previously performed the two kind of processing, and thereby save space by making the receiver circuitry more compact” (see page 2 of the Office Action and the Continuation Sheet of the Advisory Action mailed December 8, 2006).

Appellant respectfully submits that neither Ozluturk nor Sriram are directed to eliminating unnecessary components to save space. Sriram relates to reducing power consumption in the correlation co-processor by performing the requested correlation operations in stages. Ozluturk relates to a coherent demodulation system that reduces the air capacity of the global-pilot and assigned-pilot signals while maintaining the desired air-interface performance (col. 2, lines 3 to 6). That is, it is respectfully noted that both Ozluturk and Sriram **do not disclose or suggest a more compact device or eliminating circuitry.**

On the other hand, page 2, lines 4 to 20 of the specification, clearly disclose the problem of over-dimensioning a receiver and reducing the number of components required for the symbol rate processing and the chip rate processing. In other words, it is Appellant’s position that the teachings of the present invention are being used against its teacher. That is, it is respectfully submitted that the Examiner improperly relied **on Appellant’s disclosure** to provide the needed motivation. But for the present invention, one of ordinary skill in the art would not have combined the references in the manner suggested by the Examiner. Accordingly, the combination of Sriram and Ozluturk is **a creature of impermissible hindsight**. Therefore, the Examiner has not met the first requirement in establishing a *prima facie* case of obviousness.

***The Combined Disclosure of Sriram and Ozluturk do not disclose or suggest a processor performing symbol rate processing and at least a portion of chip rate processing***

The Examiner concedes that Sriram does not disclose or suggest a processor as claimed in the independent claims 1 and 9-12. The Examiner, however, alleges that Ozluturk cures the deficient teachings of Sriram and discloses a single processor performing both the signal rate processing and at least a portion of chip rate processing.

Ozluturk discloses a receiver 29 that includes a demodulator 57a, 57b which mixes down the transmitted broadband signal 55 into an intermediate carrier frequency 59a, 59b. A second down conversion reduces the signal to baseband. The QPSK signal is then filtered 61 and mixed 63a, 63b with the locally generated complex pn sequence 43a, 43b which matches the conjugate of the transmitted complex code. Only the original waveforms which were spread by the same code at the transmitter 27 will be effectively despread. Others will appear as noise to the receiver 29. The data 65a, 65b is then passed onto a signal processor 59 [sic] (depicted as signal processor 67 in Fig. 2) where FEC decoding is performed on the convolutionally encoded data (Fig. 2; col. 3, lines 41 to 53). In other words, in Ozluturk, the signal is despread prior to being input into the signal processor 59(67). That is, chip rate processing is not performed by the digital processor 59(67) but is performed prior to the signals reaching the digital processor.

Specifically, Examiner relies on col. 4, lines 12 to 14 of Ozluturk for meeting these unique features of the independent claims (*see* page 2 of Final Office Action and Continuation Sheet of the Advisory Action). Col. 4, lines 1 to 15 of Ozluturk recites:

When the signal is received and demodulated, the baseband signal is at the chip level. Both the I and Q components of the signal are despread using the conjugate of the pn sequence used during spreading, returning the signal to the symbol

level. However, due to carrier-offset, phase corruption experienced during transmission manifests itself by distorting the individual chip waveforms. If carrier-offset correction is performed at the chip level, it can be seen that overall accuracy increases due to the inherent resolution of the chip-level signal. Carrier-offset correction may also be performed at the symbol level, but with less overall accuracy. However, since the symbol rate is much less than the chip rate, less overall processing speed is required when the correction is done at the symbol level.

That is, the above-quoted passage of Ozluturk discloses that **the carrier offset may be performed at a chip level** resulting in increased accuracy **or at the symbol level** which would result in less processing. In other words, the above-quoted passage of Ozluturk relates to **when to determine a carrier offset** and **not to the chip rate processing and the symbol rate processing**. Ozluturk does not disclose or suggest that the chip rate processing is performed by the processor but in the above-quoted passage discusses various pros and cons of performing **the offset correction** at the chip level and at the symbol level. In short, the above-quoted passage of Ozluturk does not disclose or suggest a processor performing both symbol rate processing and at least a portion of chip rate processing.

Furthermore, with respect to the embodiment of Fig. 2, Ozluturk clearly discloses that the receiver 29 includes a demodulator 57a, 57b which mixes down the transmitted broadband signal 55 into an intermediate carrier frequency 59a, 59b. A second down conversion reduces the signal to baseband. The QPSK signal is then filtered 61 and mixed 63a, 63b with the locally generated complex pn sequence 43a, 43b which matches the conjugate of the transmitted complex code. "Only the original waveforms which were spread by the same code at the transmitter 27 will be effectively despread. Others will appear as noise to the receiver 29. The

data 65a, 65b is then passed onto a signal processor 59 where FEC decoding is performed on the convolutionally encoded data” (col. 3, lines 42 to 53). That is, the signal processor receives despread digital data 65a and 65b for FEC decoding.

In other words, in Ozluturk, the signal is despread prior to being input into the signal processor 59 (67). That is, chip rate processing is not performed by the digital processor but is performed prior to the signals reaching the digital processor. Moreover, in Ozluturk, the signal processor 59 (67) only performs forward error correction (FEC), which is decoding of the encoded data (col. 3, lines 51 to 53). Ozluturk, similar to the conventional technique’s described in the background of the invention and Sriram, discloses a receiver with a signal processor for performing only the symbol rate processing (Fig. 2), whereas the chip rate processing is performed by elements such as channel despreaders (depicted as elements 43a and 43b in Fig. 2) prior to the decoding by the signal processor. In short, Ozluturk is no different from the processor disclosed in Sriram or from the processor disclosed in the background of the invention and as such clearly fails to cure the deficient teachings of Sriram.

The Examiner further alleges that the embodiment depicted in Figs. 12 and 13 of Ozluturk disclose the unique features of these independent claims (*see* page 7 of the Office Action). Appellant respectfully submits that Fig. 12 of Ozluturk clearly shows the symbols entering the processor 157. That is, the chip rate processing has already been performed to return the signals to their symbol state *i.e.*, prior to the symbols entering the processor 157. For example, the signals have been despread by the despreaders 85<sub>1</sub> to 85<sub>n</sub> depicted in Figs. 11 and 13 (col. 6, lines 38 to 65 and col. 7, lines 25 to 30).

Therefore, a digital processor that can perform both symbol rate processing and at least a portion of the chip rate processing, as set forth in some variation in the independent claims 1 and 9-12 is not suggested by the combined teachings of Sriram and Ozluturk, which lack having a digital processor execute at least a portion of the chip rate processing. Therefore, the Examiner did not meet the third requirement in establishing a *prima facie* case of obviousness.

### ***Concluding Remarks***

In summary, Appellant respectfully submits that one of ordinary skill in the art would not have been motivated to combine the references in the manner suggested by the Examiner without exercising impermissible hindsight. Furthermore, the combined disclosures of Sriram and Ozluturk do not suggest the unique features of claims 1 and 9-12 discussed above. Ozluturk despreads the signals *i.e.*, performs the chip rate processing, prior to providing them to the processor, which only performs the symbol rate processing. For at least these exemplary reasons, claims 1 and 9-12 are patentable over Sriram in view of Ozluturk. Accordingly, Appellant respectfully requests the honorable Board to reverse this rejection of claims 1 and 9-12. Claims 3, 6-8, 13, and 19 are patentable at least by virtue of their dependency on claim 1 or 12.

### **Issue 2: Claims 2, 14, and 16 are Patentable over Sriram and Ozluturk in view of Warty.**

Claims 2, 14, and 16 are improperly finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Sriram and Ozluturk in view of U.S. Patent No. 4,827,499 to Warty (hereinafter “Warty”).

Of these rejected claims 2, 14, and 16, claim 2 depends on claim 1 and claims 14 and 16 depend on claim 12. It was already demonstrated that the combined teachings of Sriram and

Ozluturk fail to teach or suggest a digital signal processor configured to perform a symbol rate processing and at least parts of a chip rate processing. Warty is cited only for its teachings of processors performing task allocation (*see* page 4 of the final Office Action). Clearly, Warty does not cure the deficient teachings of Sriram. Together, the combined teachings of these references would not have (and could not have) led the artisan of ordinary skill to have achieved the subject matter of claims 1 and 12. Since claims 2, 14, and 16 dependent upon claim 1 or 12, they are patentable at least by virtue of their dependency.

**Issue 3: Claims 4, 5, and 15 are Patentable over Sriram Ozluturk, and Warty, in view of Komara.**

Claims 4, 5, and 15 are improperly finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Sriram, Ozluturk and Warty in view of U.S. Patent No. 6,161,024 to Komara (hereinafter “Komara”).

Of these rejected claims 4, 5, and 15, claims 4 and 5 depend on claim 1 and claim 15 depends on claim 12. Applicant has already demonstrated that the combined teachings of Sriram, Ozluturk, and Warty fail to teach or suggest a digital signal processor configured to perform a symbol rate processing and at least parts of a chip rate processing. Komara is only cited for its teachings of a group of digital processors (*see* page 5 of the Office Action). Clearly, Komara does not cure the deficient teachings of Sriram, Ozluturk, and Warty.

Together, the combined teachings of these references would not have (and could not have) led the artisan of ordinary skill to have achieved the subject matter of claims 1 and 12. Since claims 4 and 5 depend on claim 1 and claim 15 depends on claim 12, they are patentable at least by virtue of their dependency.

***Additional Argument directed to Claim 5***

In addition, dependent claim 5 recites: “wherein the chip rate processing and the symbol rate processing can be distributed between sub-arrays or sub-groups of signal processors.” The Examiner concedes that Sriram, Ozluturk, and Warty fail to disclose or suggest the unique features of claim 5. In addition, the Examiner appears to concede that Komara fails to disclose these unique features of claim 5 (*see* page 5 of the final Office Action).

Appellant respectfully submits that the prior art of record fails to disclose or suggest the unique features of claim 5. For example, Komara discloses a number of DSPs (18-1-1, 18-1-2, ... 18-1-p). These DSPs, however, are not split into groups such that one group performs chip rate processing and another group performs symbol rate processing. In short, Sriram, Ozluturk, Warty, and Komara, taken alone or in any conceivable combination, fail to disclose or suggest the unique features of claim 5. For at least these additional exemplary reasons, claim 5 is patentable over the prior art of record.

**Issue 4: Claims 20-24 are Patentable over Ozluturk in view of Subramanian**

Claims 20-24 are improperly finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Ozluturk in view of U.S. Publication No. 2001/0034227 to Subramanian et al. (hereinafter “Subramanian”).

***i. Arguments directed to Claims 22 and 23***

It is respectfully noted that claims 22 and 23 cannot be obvious over Ozluturk and Subramanian and this rejection is improper. Claims 22 and 23 depend on claim 1 and as such contain all the features of claim 1. If the Examiner deemed necessary to reject claim 1 as being obvious over Sriram in view of Ozluturk (that is, Sriram is necessary to meet the unique features

of claim 1), then claims 22 and 23 cannot be rejected as being obvious over just Ozluturk and Subramanian.

Furthermore, it is respectfully submitted that Subramanian is being cited only for its disclosure of the switching means (*see* page 5 of the final Office Action and the Continuation Sheet of the Advisory Action). Clearly, Subramanian does not cure the deficient teachings of Sriram and Ozluturk. Together, the combined teachings of these references would not have (and could not have) led the artisan of ordinary skill to have achieved the subject matter of claim 1. Since claims 22 and 23 depend on claim 1, they are patentable at least by virtue of their dependency.

In addition, dependent claim 22 recites: “each of said digital signal processors is configured to perform the symbol rate processing comprising decoding the received information and at least said parts of the chip rate processing comprising despreading the received information.”

As explained above, Ozluturk only discloses that the carrier offset may be performed at a chip level resulting in increased accuracy or at the symbol level which would result in less processing. With respect to the processor 59 (67), Ozluturk only discloses that the original waveforms which were spread by the same code at the transmitter 27 will be effectively despread. Others will appear as noise to the receiver 29. The data 65a, 65b will then be passed onto a signal processor 59 where FEC decoding (col. 3, lines 42 to 53). That is, the signal processor receives the despread digital data 65a and 65b for FEC decoding. In other words, in Ozluturk, the signal is despread prior to being input into the signal processor 59 (67). In short, the digital signal processor 59 (67) does not perform the decoding of the received information

and the despreding of the received information. Subramanian does not cure the deficient teachings of Ozluturk. For at least these additional exemplary reasons, claim 22 is patentable over Ozluturk in view of Subramanian.

In addition, dependent claim 23 further recites that the despreding comprises separating the received information based on sources of the received information and assigning the separated received information to a respective source. Ozluturk does not disclose or suggest the processor 59 (67) separating the received information based on sources of the received information and assigning the separated received information to a respective source.

Subramanian does not cure the deficient disclosure of Ozluturk. For at least these additional reasons, claim 23 is patentable over Ozluturk in view of Subramanian.

***ii. Arguments directed to Claims 20, 21, and 24***

Of the remaining rejected claims 20, 21, and 24, only claim 20 is independent.

Independent claim 20 *inter alia* recites: “means for switching over from said means for executing symbol rate processing to said means for executing chip rate processing, wherein the digital signal processor is a single digital processor having the symbol rate processing means, the chip rate processing means and the switching means and wherein the digital signal processor is disposed inside a receiver.” As explained above, Ozluturk does not disclose or suggest a single processor having means for executing chip rate processing and means for executing symbol rate processing. Subramanian is cited only for its disclosure of switching and as such does not cure the deficient disclosure of Ozluturk.

That is, Subramanian relates to a method of generating a configuration for a configurable spread spectrum communication device. The method is implemented on a computing device and

starts with receiving an input identifying a desired function, and a desired operation within the desired function, to be implemented by a configurable communication device. Subsequently, a signal flow path for the desired operation is generated by the computing device. Next, the desired operation is mapped onto a computing element within the configurable communication device; the computing element having localized control and being function-specific. The configurable device is configured to enable the mapping operation and signal flow path across a computing element for each of the multiple operations which together enable the desired function (*see* Abstract and ¶¶ 9 through 11).

In other words, Subramanian discloses a complex computing device which generates a signal flow path and maps it onto various configurable elements of the configurable device. This computing device needs its own processor, memory, and user interface. In other words, Subramanian does not disclose or suggest having a single processor perform the chip rate processing, the symbol rate processing, and the switching. In Subramanian, a separate external computing device 102 with a memory and a user interface is provided to map out the signal flow (element 102 in Fig. 1A and Fig. 2; ¶¶ 21 and 30). Then, the mapped out signal flow is transferred to the configurable device 104 for implementation (Fig. 1; ¶¶ 22 and 24). In other words, Subramanian clearly discloses separate devices for the spectrum processing and for the switching.

In short, Subramanian does not disclose or suggest the switching means within the signal processor. That is, Subramanian does not disclose or suggest the separate, external computing device being provided in a signal processor of a receiver, as recited in claim 20. Subramanian clearly does not cure the deficient disclosure of Ozluturk.

Moreover, one of ordinary skill in the art would not have been motivated to combine the references in the manner suggested by the Examiner. The Examiner contends that one of ordinary skill in the art would have been motivated to combine the references for most effective processing based on the type of processing required at any given time (*see* pages 5 and 6 of the Office Action and page 2 of the Continuation Sheet).

However, in Ozluturk, separate elements are provided for the symbol rate processing and the chip rate processing. In Ozluturk, there is no need to having a switch for switching between the two. That is, since separate elements are provided for each type of processing, these processes can be performed concurrently and the switch is not needed. Moreover, in Ozluturk, there is no disclosure or suggestion that some of the elements should be bypassed. Therefore, the proposed combination would not provide more effective processing.

Furthermore, the proposed combination is unworkable. An external computing device of Subramanian (with the memory, the processor, and the user interface) cannot be placed in the processor 59 (67) of Ozluturk. That is, one of ordinary skill in the art would not have and could not have placed an external computing device that includes a memory, a processor, and a user interface into the processor 59 (67) of Ozluturk. In short, one of ordinary skill in the art would not have and could not have combined the two references in the manner suggested by the Examiner.

Therefore, “means for switching over from said means for executing symbol rate processing to said means for executing chip rate processing, wherein the digital signal processor is a single digital processor having the symbol rate processing means, the chip rate processing means and the switching means and wherein the digital signal processor is disposed inside a

receiver,” as set forth in claim 20 is not obvious in view of the combined teachings of Ozluturk and Subramanian, which lack a single processor having the symbol rate processing means, the chip rate processing means, and the switching means. For at least these exemplary reasons, independent claim 20 is patentable over Ozluturk in view of Subramanian. Accordingly, Appellant respectfully requests the Board to reverse this rejection of claim 20 and its dependent claims 21 and 24.

*iii. Additional Arguments directed to Claim 21*

In addition, dependent claim 21 recites: “wherein the means for switching instructs for transmission of information in the digital processor first to the means for executing chip rate processing and then to the means for executing symbol rate processing.” As acknowledged by the Examiner, Ozluturk does not disclose or suggest the switching means (*see* page 5 of the final Office Action). Subramanian does not cure the deficient disclosure of Ozluturk. Subramanian simply discloses that an external configuration device may create a system data flow and transfer the created data flow onto the configurable device 104 for implementation. Some of the processes that may be performed include chip despread and channel decoding (¶¶ 22, 24, and 42). Although Subramanian discloses creating a signal flow and transferring the signal flow to the configurable device 104, Subramanian does not disclose or remotely suggest having the switching means first transfer the signal to the chip rate processing means of the signal processor and then transferring the signal to the symbol rate processing means of that same signal processor. In short, Subramanian does not cure the above-identified deficiency of Ozluturk. For at least these additional exemplary reasons, claim 21 is patentable over Ozluturk in view of Subramanian.

*iv. Additional Arguments directed to Claim 24*

Dependent claim 24 recites “said symbol rate processing means decode the received information and wherein said chip rate processing means despread the received information.” In Ozluturk, the data is despread and then FEC decoded. In other words, Ozluturk discloses the data 65a and 65b passing to the signal processor 59 (67) where FEC decoding is performed (col. 3, lines 48 to 53). Ozluturk does not disclose or suggest the signal processor 59 (67) having means for decoding the received information and means for despread the received information. Subramanian does not cure the above-identified deficiencies of Ozluturk. For at least these additional exemplary reasons, claim 24 is patentable over Ozluturk in view of Subramanian.

**Concluding Remarks**

In view of the above, Appellant respectfully requests the Board to reverse the rejections of claims 1-16 and 19-24.

APPEAL BRIEF UNDER 37 C.F.R. § 41.37  
U.S. Appln. No. 09/981,784  
Attorney Docket No.: Q66664

**VIII. CONCLUSION**

The statutory fee of \$500.00 is being paid via the USPTO Electronic Filing System (EFS). The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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**CLAIMS APPENDIX**

**CLAIMS 1-16 AND 19-24 ON APPEAL:**

1. A base station of a radio-operated telecommunications system comprising:  
  
a receiver processing received information; and  
  
one or more digital signal processors, wherein each of said digital signal processors is configured to perform a symbol rate processing and at least parts of a chip rate processing.
2. The base station as claimed in Claim 1, wherein the signal processor is also configured to perform a task allocation for controlling the chip rate processing and the symbol rate processing.
3. The base station as claimed in Claim 1, the signal processor being designed such that firstly the chip rate processing and then the symbol rate processing can be performed.
4. The base station as claimed in Claim 1, wherein an array or group of digital signal processors is provided.
5. The base station as claimed in Claim 4, wherein the chip rate processing and the symbol rate processing can be distributed between sub-arrays or sub-groups of signal processors.
6. The base station as claimed in Claim 1, wherein at least one memory is provided which is suitable for and provided for the intermediate storage of the received information.

7. The base station as claimed in Claim 1, wherein the chip rate processing comprises a despreading of the received information and wherein the signal processor is configured to dispread the received information.

8. The base station as claimed in Claim 1, wherein the symbol rate processing comprises a decoding of the received information.

9. A receiver for a base station of a radio-operated telecommunications system for processing received information with one or more digital signal processors, wherein each of said digital signal processors is configured for performing a symbol rate processing and at least parts of a chip rate processing.

10. A digital signal processor configured to execute symbol rate processing for a receiver of a base station of a radio-operated telecommunications system, wherein the signal processor is configured to perform at least parts of a chip rate processing.

11. A radio-operated telecommunications system comprising at least one of:  
a base station having one or more digital signal processors, wherein each of the digital signal processors is configured to perform a symbol rate processing and at least parts of a chip rate processing;

a receiver processing received information having said one or more digital signal processors; and

said one or more digital processors.

12. A process for operating a radio-operated telecommunications system, wherein information received by a base station is subjected to a symbol rate processing by one or more digital signal processors, wherein at least a part of the chip rate processing is performed by same processor from the digital signal processors.

13. The process as claimed in Claim 12, wherein firstly the chip rate processing and then the symbol rate processing is performed.

14. The process as claimed in Claim 12, wherein a task allocation for controlling the chip rate processing and the symbol rate processing is performed by the at least one signal processor.

15. The process as claimed in Claim 12, wherein an array or group of digital signal processors is provided, the chip rate processing and the symbol rate processing is distributed between sub-arrays or sub-groups of signal processors.

16. The process as claimed in Claim 15, wherein the distribution of the array or group of signal processors between the chip rate processing and the symbol rate processing is performed by the task allocation.

19. The telecommunication system according to claim 11, wherein the telecommunication system is a code division multiple access (CDMA) telecommunications system.

20. A digital signal processor comprising:  
means for executing symbol rate processing;  
means for executing chip rate processing; and  
means for switching over from said means for executing symbol rate processing to said means for executing chip rate processing,

wherein the digital signal processor is a single digital processor having the symbol rate processing means, the chip rate processing means and the switching means and wherein the digital signal processor is disposed inside a receiver.

21. The digital signal processor according to claim 20, wherein the means for switching instructs for transmission of information in the digital processor first to the means for executing chip rate processing and then to the means for executing symbol rate processing.

22. The base station according to claim 1, wherein each of said digital signal processors is configured to perform the symbol rate processing comprising decoding the received information and at least said parts of the chip rate processing comprising despread the received information.

23. The base station according to claim 22, wherein said despread comprises separating the received information based on sources of the received information and assigning the separated received information to a respective source.

24. The digital signal processor according to claim 20, wherein said symbol rate processing means decode the received information and wherein said chip rate processing means despread the received information.

APPEAL BRIEF UNDER 37 C.F.R. § 41.37  
U.S. Appl. No. 09/981,784  
Attorney Docket No.: Q66664

**EVIDENCE APPENDIX**

NONE

APPEAL BRIEF UNDER 37 C.F.R. § 41.37  
U.S. Appl. No. 09/981,784  
Attorney Docket No.: Q66664

**RELATED PROCEEDINGS APPENDIX**

NONE